WHEN TO USE AOI, WHEN TO USE AXI, AND WHEN TO USE BOTH

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ABSTRACT

With today's technology embracing ever-smaller chip components, array packages with hidden solder joints, and numerous components on both sides of the printed circuit board assembly (PCBA), manual visual inspection is running out of steam to adequately address these challenges. AOI (automatic optical inspection) and/or AXI (automatic X-ray inspection) are starting to be used at a majority of today's manufacturing sites. The key question is: When is it best to use AOI, when to use AXI, and when to use both?

This paper will answer that question by addressing several issues for selecting the best inspection strategy. The paper will present data from many studies Agilent has performed in the quest to find the optimal test / inspection strategy. The paper will also make recommendations on which of these strategies to use in different situations.

INTRODUCTION

"When to use AOI, when to use AXI, and when to use both?" is unfortunately not an easy question to answer. It is not a simple matter of looking at just a few characteristics and then having the answer. The reality is significantly more complex, and there are many factors to consider to get even close to an answer. This paper attempts to share data and new thoughts on this question. Please see it more as guiding principles than absolute truth.

Today's test engineers have significantly more challenges than just a few years ago. The board complexity is increasing with more components, more joints, higher densities, new package technologies such as area array packages, and 0402 and 0201 chip components. The higher component and joint counts create more defect opportunities which lead to lower yields for a given defect level. At the same time, there are more test and inspection alternatives today with new technologies such as Solder Past Inspection (SPI), Automatic X-ray Inspection (AXI), and Automatic Optical Inspection (AOI). These inspection technologies are well established and provide real choices among capabilities and benefits. Boundary-Scan test technology has also emerged as a popular electrical technique to complement In-Circuit Test (ICT) and Functional Test (FT). While these new tools offer more choices, they also pose a new dilemma. Which is the right test / inspection strategy? Which is the right combination of these tools?

This paper will focus on the selection of AOI and / or AXI. Today, most test engineers have a good understanding of the optimal use of ICT, Boundary-Scan and Functional Test. It is assumed that these test strategies are used to complement the major inspection strategies discussed in this paper. It is also outside the scope of this paper to discuss Solder Paste Inspection (SPI) in detail.

The main focus of this paper is selecting inspection strategies for volume production. Prototype testing poses unique challenges because of the need for fast test/inspection turn-around times for program development and the typically low quantities of boards manufactured. Prototype testing strategies are outside the scope of this paper.

Key words: Automatic Optical Inspection (AOI), Automatic X-ray Inspection (AXI), Test / inspection strategy, Defect Containment, Process Control, Test Effectiveness.

METHODOLOGY

The results and suggestions presented in this paper come from many different studies and research activities. Some of the key insights emerged from test effectiveness studies [1] and studies of overall effectiveness when a combined strategy of x-ray test and simplified ICT test are evaluated [2]. Both types of studies are performed in a very similar way. Typically, between 20 and 100 printed circuit board assemblies (PCBAs) are included in each study. These boards are inspected and tested by different types of test and inspection equipment. The equipment user, whether Contract Manufacturer (CM) and/or their OEM customer, classify all defects as true defects or false calls. One key aspect of these studies is that defects are not repaired until the last test or inspection system has tested the board. By doing this, all test / inspection systems have an equal chance of detecting all defects, and thus a test effectiveness score can be calculated for each system. Very accurate data gathering takes place at these studies.

An important question to ask is where in the production line are defects introduced? A related follow-up question is, Do defects originating early in the manufacturing process self-correct, so that at the end of the production line they do not constitute a defect? To gain some insight into these questions an ambitious study was undertaken. In this study, several points of examination were included: AOI pre-reflow, AOI post-reflow, AXI pre-wave, AXI post-wave, and ICT. Again, no defects were repaired during the flow through the manufacturing steps but a very careful and accurate recording was made of all defects.

Industry defect levels are also an important factor when discussing test strategies. An extensive study of fifteen companies' defect levels was done and presented in a paper[3]. In this study these fifteen companies provided production data from automated X-ray inspection (AXI) and the repair information after the inspection.

RESULTS AND INSIGHTS TO KEY FACTORS

Defect and process indicators

The term defect is used extensively throughout this paper and should be defined. "A defect is an unacceptable deviation from a norm." The key word in this definition is "unacceptable." Assuming the defect is identified, if it is unacceptable to the manufacturer, some corrective action is taken and the defect removed. Another way to say this is, "A defect is an issue with the board that, once detected, would stop shipment of the unit until corrective action is taken."

A process indicator is either an "acceptable deviation from the norm" or a "defect" early in the process that is self correcting. For the first case a good example is an insufficient solder joint. It is not so insufficient as to require a touch-up, but it is valuable process information especially if many of these process indicators are seen for one solder joint location. An example of the other type of process indicator is a pre-reflow misaligned component that aligns itself during reflow. After reflow it is no longer a defect. It is very important to acknowledge that information about process indicators can be very valuable. With this information, process engineers can take corrective action and improve the process, resulting in fewer defects at the end of the manufacturing line.

Defect levels in the industry

One of the frequent claims made in the industry is that companies have defects at the rate of only 50 – 100 Parts Per Million (PPM) or Defects Per Million Opportunities (DPMO). Our observations suggest that these defect levels are probably obtained only on the board types with the lowest defect levels and probably only on a "good" day when everything is working to the advantage of that company. The average actual defect levels are typically significantly higher. A key point is that optimal test strategy is very different if the general defect levels are around 50 DPMO versus 500 DPMO. A very comprehensive study [3], with production data from about six months of production at fifteen different companies and over one billion solder joints in the study indicated an average defect level of between 650 to 1,100 DPMO. These numbers are probably closer to the real defect numbers in the industry, especially on medium and high complexity boards that are manufactured in smaller batches. Board types manufactured in higher volumes on the same SMT line for several days typically have lower defect levels, between 200 DPMO to 600 DPMO, because process adjustments can be made to achieve lower defect levels.

The DPMO levels are stated here on a joint basis. One solder joint is one defect opportunity and there can be either zero or maximum one defect per solder joint. Sometimes DPMO data is calculated on a per component basis or on a board basis. Because the values are significantly different, these should not be used for comparison. For instance the defect level per joint in this study is 1,100 DPMO(j). The board-level defect reading of the same data is 376,600 DPMO(b), a significant difference. It is recommended to indicate defect levels on a joint basis DPMO(j) or PPM(j). For defect levels on a component basis, the notation DPMO(c) or PPM(c) is used; likewise the board level notation is DPMO(b) or PPM(b).

In addition to knowledge about defect levels, it is also important to have knowledge of where in the manufacturing process that defects are introduced and can be detected. Much of this knowledge has been gained through Test Effectiveness studies, so this will be addressed in the next section.

Test Effectiveness studies

If we agree that defect levels are typically higher than commonly claimed, next we need to address the test effectiveness of major inspection and test technologies, through a Test Effectiveness study. This study is done on a smaller sample of boards, typically between 20 to 100 boards. The lower number is used if the study is done on a very complex board with many defect opportunities. The higher number of boards is used for medium complexity boards with fewer defect opportunities. For optimum results a total of 100 to 200 defects should be found. The same set of boards is tested / inspected by different methods, such as AOI and / or AXI, ICT, and sometimes Functional Test.

For example, if we are doing a Test Effectiveness study of AOI, AXI, ICT and Functional Test, the boards are first inspected by the AOI system. All calls that the AOI system makes are classified as either true defects or false calls. A log is kept of all defects classified as true defects, but they are not repaired at this time. Typically only one defect per component is counted, even if, for example, one QFP component has five open pins. After AOI the boards go to the AXI system and we repeat the process. All AXI calls, classified as true defects, are noted in the log. Again no repairs are done at this time. Typically many of the defects found by the AOI system are also found by the AXI system. There are usually a few defects detected by the AOI system that the AXI system did not detect; however there are typically many defects found by AXI that AOI did not detect.

After AXI the boards go to the ICT system and are tested again. At this stage some defects must be repaired, such as solder bridges, so the analog ICT measurements can be done properly and there is no danger in powering up the board. However we try to minimize the ICT repair when the Functional test is part of the study. Again at ICT we are trying to isolate the true defects from false calls. After ICT

the boards go to Functional Test and the process repeats. Since Functional Test is the last step in our example study, we can now start to do repairs. In a Test Effectiveness study we are only keeping track of defects, and not of process indicators. It is also important to note that it is not the engineers representing the ATE vendor (Automatic Test Equipment) that makes the judgment on what is a defect and what is not. This is done by the CMs' and / or OEMs' engineers.

When doing repairs at Functional Test and classifying the defects at ICT we leverage what we have learned at AOI and AXI. For example if AOI and AXI have identified a missing resistor, let's say a 1K Ohm resistor and ICT measures this resistor as a very high value M Ohms instead of around 1K Ohm we know that ICT has found the same defect. In most cases, a retest of the boards at Functional Test and ICT is necessary after repairs, to make sure all defects have been correctly identified and repaired. All defects detected by AOI and AXI and not detected by ICT and Functional Test are also repaired at this time.

Let's assume that after this process we have found a total of 100 defects. Let's also assume the AOI system found 60 of those defects, the AXI system found 90 of the defects, the ICT system 40 and the Functional test 30. Then the AOI system's Test Effectiveness is 60% (60 out of a total of 100 known defects), the AXI Test Effectiveness is 90%, the ICT 40% and the Functional Test 30%.

Generally a Test Effectiveness study takes 3 to 5 working days to perform, not including any program preparation that may be needed. It is very important to keep very good track of each defect, and it is better to limit the number of boards in the study than to compromise the integrity of the data. A Test Effectiveness study, executed correctly, is almost always a big eye opener and is strongly recommended to do every third or fourth year or when any new, significant changes in test strategy are considered.

Test Effectiveness Case Study [1]

The effectiveness of each test / inspection system will vary from shop to shop and even from assembly type to assembly type. The data presented in this paper is being shared in an attempt to show the usefulness of a Test Effectiveness study and to share some insights on effectiveness and where defects are introduced in the manufacturing process.

This first data is a compilation of two Test Effectiveness studies. These two studies included AOI post-reflow, AXI, and ICT. In these two cases, no hand-load and solder wave process were included, therefore AOI, AXI, and ICT were all at the same manufacturing process. In these two studies there were a total of 80 boards inspected / tested and a total of 200 defects identified by the systems and confirmed by the CM. AOI was able to detect 127 out of the total of 200 defect, resulting in a test effectiveness of 64%. AXI was able to detect 163 defects, resulting in a test effectiveness of 82%. ICT found 116 of all defects, resulting in a test effectiveness of 58%. Figure 1 shows the test effectiveness for AOI post-reflow, 3D AXI, and ICT.

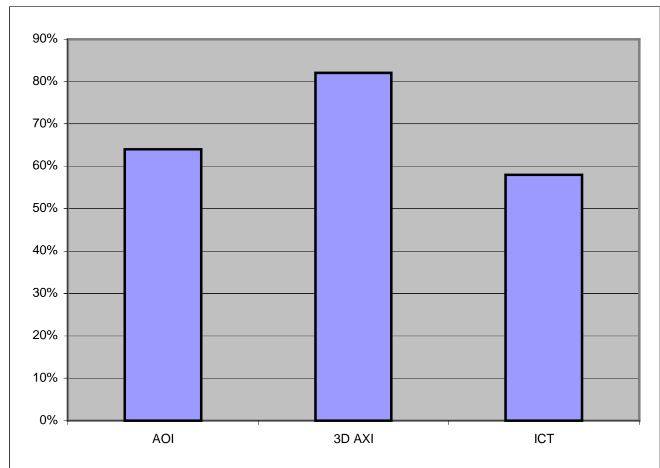

Figure 1. Case Study 1, test effectiveness for AOI post-reflow, 3D AXI, and ICT.

Test Effectiveness Case Study [2]

This study was performed to compare AOI to AXI and also to gain some insights on where the optimal placement of these inspection systems would be, depending on where defects were introduced. It should be noted that this study is focused on detecting defects that are also defects at the end of the manufacturing line. The study is not trying to gain insights into how test and inspection can be used to improve the process. The current test strategy includes ICT. The AOI, AXI, and ICT were performed after the following process steps (see table 1).

Process step	AOI	AXI	ICT
Post pick-and-place, Pre-reflow	X		
Post-reflow, Pre-wave	X	X	
Post-wave		X	X

Table 1

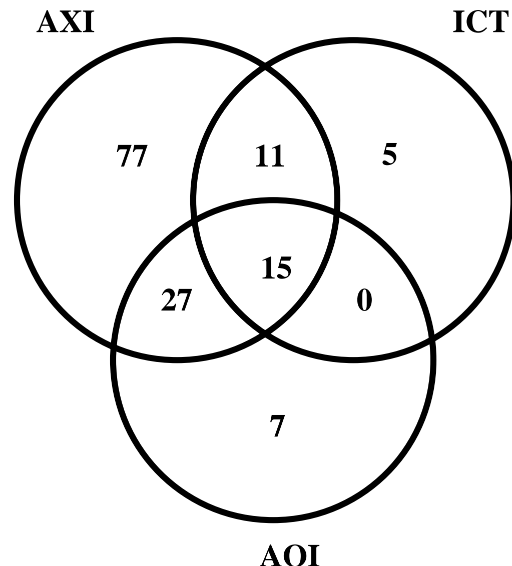

Figure 2. Defects found by AOI, AXI, and ICT.

The first data is presented in Figure 2, a Venn diagram showing the defect coverage for each tester. The AOI circle represents all defects found by the AOI at both inspection points. Likewise the AXI circle includes any defect found at either AXI step.

We can see that the current test strategy, ICT is only catching 22% of all defects. Adding AOI to this test process will increase the test effectiveness to 46%. Or adding AXI to ICT will increase the test effectiveness to 95%.

Next we look more closely at the AOI and AXI results at each process step. Figure 3 shows a Venn diagram breakdown by defects detected by AOI pre-reflow and defects detected post-reflow. From this new breakdown we can see that AOI post-reflow was more effective than AOI pre-reflow to detect final defects. It should be noted that pre-reflow AOI detected many process indicators, for instance misaligned components, that was corrected by the surface tension at the reflow process. The AOI pre-reflow could have contributed significantly at process improvements and adjustments of the placement machines.

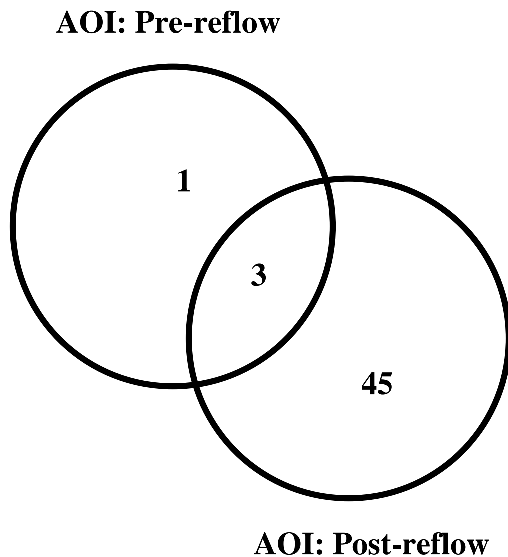

Figure 3. Defects found by AOI Pre-reflow and AOI Post-reflow. Only defects counted as defect at the end of the manufacturing line are included.

Figure 4 shows a breakdown for AXI. AXI was done both pre-wave and post-wave. Here we see that AXI is more effective post-wave than pre-wave, because the wave (or selective wave) process is introducing a significant number of defects, in this case around 40% of all defects. That should also be taken into consideration when the test effectiveness of the AOI is judged. 40% of the defects were introduced after the AOI inspection.

We have seen very similar results, that the wave process introduces significant numbers of defects, from the special test effectiveness studies we have done when analyzing a test strategy of maximum 3D x-ray with a limited or reduced ICT test [2]. In one of these studies, defects introduced at the hand-load and selective wave-process accounted for over 55% of final defects. In the other studies, we did not specifically keep track of this number but on average around 50% of all defects appear to be introduced at the wave process.

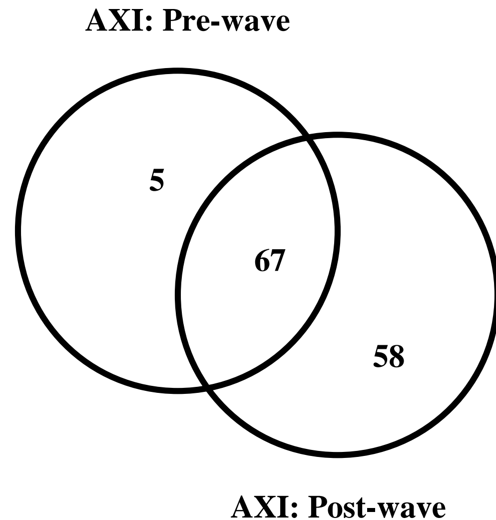

Figure 4. Defects found by AXI Pre-wave and AXI Post-wave. Only defects counted as defect at the end of the manufacturing line are included.

These case studies illustrates that a significant number of defects are detectable only after reflow and also that the wave or selective wave introduces almost half of all defects. It highlights the importance of good defect containment as late as possible in the manufacturing line.

The studies we have performed have mainly been focused on defect containment. We have only counted defects that were still defects at the end of the manufacturing line. However we have noticed a significant number of process indicators in these studies.

Where in the manufacturing process are defects introduced?

As discussed in the previous section, the reflow oven can be seen as a defect transformation box. Many defects go in into the reflow oven and many defects come out from the reflow oven, but they may not always be the same ones. Examples of defects that change are: misaligned parts that self-align, insufficient solder that can make acceptable joints, parts that fall off, apparently good parts that do not solder, solder bridges that open up, and open areas that get bridged. At the same time some defects are the same both before and after the reflow oven. Examples are: missing parts that are still missing, parts with no solder paste that will not solder and will be open, gross misalignments that will still be misaligned, reversed parts that will still be backwards, and some misaligned that are still misaligned. So for defect containment it is best to place the AOI system after the reflow oven. For optimal process control and for repair of

expensive components the optimal AOI system position is pre-reflow.

We also saw in the previous section that a wave or selective wave process contributes around 50% of all defects. For this reason it is best to place the inspection system after the wave process for maximum defect containment.

Field failures and warranty costs

It is obvious that the selected test / inspection strategy will have an impact on the number of defects found by the end customer and also on warranty costs. An analysis of real production data done by a Hewlett-Packard division shows higher yields into Functional Test, and fewer field returns if an efficient inspection strategy is used to complement ICT and Functional Test. The following is data gathered within HP that shows the effectiveness of the combination of AXI and ICT before Functional Test. This HP division uses a Contract Manufacturer (CM) for their board manufacturing. The CM can provide manual visual inspection (MVI), AXI, and ICT, while the HP division does its own Functional Test. Each PCBA has a unique serial number and field failures are also tracked, using these unique serial numbers.

This data is not an experiment, but data gathered from normal production and field failures over a significant amount of time. The 6,928 boards in this study are of the type high mix – low volume.

Six different board types are included in the data. For one board type no AXI or ICT was performed, only minimal MVI, due to lower anticipated lifetime volume and lower complexity. For five board types ICT was used. However very good experience with the combination of AXI and ICT made them add AXI to all of these five board types. Table 2 shows how many boards are in each group. (See Table 2 at the end of this paper)

Capability to detect solder defects. In Table 2, you can see each major test strategy's effectiveness at detecting solder-related defects. The DPMO(c) levels reported are defects detected at Functional Test. DPMO(c) is Defects Per Million Component Opportunities. If only MVI was used, Functional Test saw 419 DPMO(c) solder defects. If ICT was added this number was reduced to 195 DPMO(c), and if a combination of AXI and ICT was used this number was reduced to 23 DPMO(c). In this study no data is available for the effectiveness of AXI alone, but experience and references mentioned earlier indicate that AXI is extremely effective in finding solder-related defects.

Capability to detect non-solder-related defects. Table 2 indicates the different strategies' effectiveness in detecting non-solder-related defects. If only MVI is used 382 DPMO(c) are detected at Functional Test. If ICT is added the defect level decreases to 192 DPMO(c). If both AXI and ICT are used the defect level basically stays the same at 195 DPMO(c). This is not to surprising since AXI is not well suited to detect non-solder-related defects. It also illustrates the value of ICT and Functional Test as a complement to a good inspection strategy.

Capability to reduce field failures. In Table 2 the field failures can be seen for boards that have gone through the different test strategies. The boards that have only been visually inspected and functionally tested have a field failure rate of 33 DPMO(c). If ICT has been added this decreases to 20 DPMO(c). For boards with AXI, ICT, and Functional Test, the field failure rate is down to 3 DPMO(c) for this sample of boards. This is almost an order of magnitude reduction in field returns. Other users have seen similar results. This is quite significant and can be converted to significant savings in warranty cost -- in many cases several million dollars per year.

Complexity

Another factor that impacts the test strategy selection is the board complexity. However the term "high complexity board" is very subjective. One company may be producing boards with over 30,000 solder joints and several thousand components on double-sided boards, while another company produces a single-sided board with fewer than 1,000 solder joints and under a hundred components. Both these companies claimed that these boards were "high complexity boards." It is obvious that the complexity of these two boards is very different. To provide a way to talk about board complexity in a more objective way, a Complexity Index was introduced in 1999 [4]. The original Complexity Index was calculated using number of components, number of joints, number of board sides, and low volume – high volume production batches. The objectives for the Complexity Index were to be very easy to calculate and to give a good indication of the complexity of the board. One key enhancement request has been that some form of component density or joint density should be included in the Index. Therefore a new, updated Complexity Index is suggested as:

$$Ci = ((\#C + \#J)/100) * S * M * D$$

Ci = Complexity Index
#C = Number of components
#J = Number of joints
S = Board sides (1 for double sided, and ½ for single sided)
M = Mix (1 for high mix, and ½ for low mix)
D = Density ((joints / square inch)/100) or
(joints / square cm / 15.5)

If the resulting Complexity Index is below 50 it is considered a low complexity board. If it is between 50 and less than 125 it is a medium complexity board, and if it is above or equal to 125 it is a high complexity board.

There are other factors that contribute to the complexity of a board, but, these key considerations kept the Complexity Index simple enough for everybody to find the numbers necessary for the calculation and then obtain the right "ball park" indication of the board's complexity. A final caveat:

this index refers to complexity from a manufacturing point of view, not from a testing point of view. In manufacturing, the higher the complexity, the more difficult it is to achieve high yields without any test and inspection. Board complexity is an important parameter when selecting test strategy.

Board complexity and board volume

In general AOI systems have higher inspection throughputs than AXI. On the other hand 3D AXI has higher test effectiveness. The higher test effectiveness is important when complexity increases. Figure 5 illustrates a general criteria for selecting which major inspection strategy to use to find defects. If the board complexity is very low and the board volume is low, MVI is probably still a good alternative. If complexity or volume increases, an AOI system should be considered. When the complexity increases, the AXI starts to be a better solution. At the far right of the figure where complexity is very high, a combination of both AOI and AXI is in most cases the most economical strategy. If we look at the volume we can see as a general guideline AXI is a good solution for low to medium board volumes and AOI is a good solution for medium to high volumes.

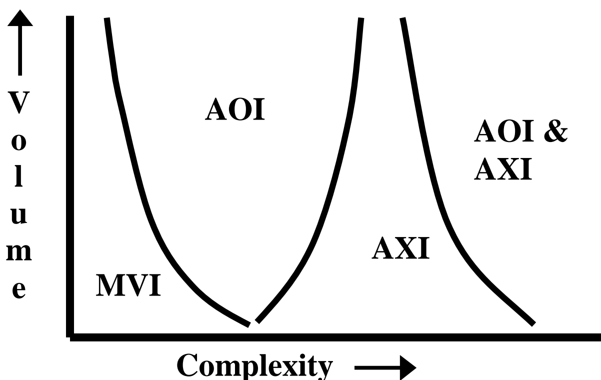

Figure 5 General recommendations of AOI and/or AXI based on board complexity and manufacturing volumes.

Process control

Test and inspection should always be used to lower variability of the manufacturing process, resulting in lower defect levels. It would be great if we could measure process improvements in a similar way we do in the Test Effectiveness studies. One way to do this would be to have two identical lines running. In one line we allow process control and process improvements. In the other line we do not allow process control and improvements. Now we run these two lines over a significant amount of time and measure the difference. Nobody has done this type of study for the obvious reason that the line without process control would have significantly higher defect levels and significantly higher costs induced by all the repairs that needs to be done in this case. In a perfect study you would not allow any process control, but all process engineers have learned a significant amount of process control and are applying this intentionally or unintentionally.

However it is easy to do economic analysis and calculate the savings if the defect levels are reduced by using the test / inspection systems to help with process control. In most cases savings of several hundred thousands dollars per year can be achieved if the DPMO(j) level is reduced by 100 – 200 DPMO(j).

To gain the maximum benefit of effective inspection, it should occur as early as possible in the manufacturing process. Solder Paste Inspection and AOI pre-reflow, make a lot of sense. At the same time if inspection is mainly used for process control it should be complemented with an efficient defect containment strategy at the end of the line. This effective defect containment also gives a complete picture of all defects and also gives a complete picture for process control.

A good data collection system is important to have in place to be able to use the data from test and inspection for process control. Also for maximum results of process control, enough engineering resources should be available to analyze the data, find the root cause, and take appropriate corrective action. Without adequate engineering resources, the gathered data will be of limited value.

So a general guideline, for process control with short feedback loops place the inspection system(s) as early as possible in the manufacturing process. On the other hand, for highest defect containment, the inspection system(s) should be as late as possible in the manufacturing process. This is illustrated in Figure 6 (see Figure 6 at the end of the paper). It is important to recognize that one strategy will not replace the need for the other strategy. For instance using inspection for process control does not eliminate the need for a good inspection or test at the end of the line for defect containment. And a good test/inspection strategy at the end of the line does not eliminate the need for early inspection for process control. A balance of these strategies needs to be in place because we have both systematic defects that can be minimized with process control, as well as random defects that need to be contained at the end of the line.

Examples

Let's look at a couple of examples and see what test strategy might be considered:

The first example is a medium-complexity, high-volume board. It has good ICT access, around 80% probe access and almost all of the nets that do not have probe access have access through boundary-scan. There are a few BGAs on the board, but they all have boundary-scan built into them. For volume production, AOI post-reflow is recommended because of the high volume and good ICT access. The AOI inspection will be followed by ICT with boundary-scan and Functional Test.

The next example is a high-complexity board that will be manufactured in medium volumes. A selective wave process

is needed for some through-hole components and connectors. The board does not have close to 100% electrical access, even though a significant number of ICs have boundary-scan. The recommended test strategy for this board is AXI after wave, followed by ICT with boundary-scan and then Functional Test. The AXI is selected in this case because of the high board complexity, and it is placed after wave since it is known that this process step introduces a significant number of defects.

This example is a very high-complexity, low volume board. The R&D engineer has indicated that he can only provide around 50% probe access. He has requested input from the test engineer to identify his preference for where probe access is needed. On this board there are a few, very expensive ICs. Before the board layout phase it is decided to use AXI with simplified ICT to address the need to remove around 50% of the test pads. A test analysis tool is used to recommend where ICT test probes are needed and where they can be eliminated. The general concept is to test for solder opens and bridges with AXI. The ICT test will follow and the main focus is to test that the right components have been placed, that they are oriented correctly and that they have basic functionality. The strategy will be complemented with AOI pre-reflow and Functional Test. The main purpose with the pre-reflow AOI is to inspect the very expensive components and make sure they are oriented and aligned correctly. Finding these types of defects before re-flow means that the expensive components can be "repaired" and reused. The AOI will also inspect other components and will also be used for process control.

The last example is a low to medium complexity board that will be manufactured in high volumes. This board type is the next generation of a board type that is already in production. The experience with the current board type is that defect levels are low. During design of the new board type significant efforts have been made to further decrease manufacturing defects. The recommended strategy for this case is to use AOI-pre-reflow. The main focus of the AOI is to use it for process control. If the process goes out of control, early detection is possible and corrective actions can be taken before too many additional boards are manufactured. The pre-reflow AOI will also provide early detection of defects that can be detected at this stage. After reflow the test strategy is ICT and Functional Test.

CONCLUSIONS AND SUMMARY

AOI and AXI are today valid options as inspection alternatives to Manual Visual Inspection and are used widely in the industry.

Today there are many test / inspection strategies making it more complex to select the optimum combination.

Defect levels in the industry are significantly higher (500 to 1,000 DPMO(j)) than typically acknowledged in the industry.

In all Test Effectiveness studies performed 3D AXI has been found to have the highest Test Effectiveness. The second most effective test / inspection technique is AOI.

A number of defects change during reflow.

A significant number of defects (around 50%) are introduced by the hand load and wave or selective wave process.

A good inspection strategy can reduce the number of field failures and lower warranty costs.

Board complexity and manufacturing volumes are important factors when selecting inspection strategy, but they are not the only factors.

A combination of inspection strategies for process control and defect containment should be in place.

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Activities prior to Functional Test	Number of boards	Faults found at Functional Test			Field failures DPMO(c)
		Solder defect DPMO(c)	Non-Solder DPMO(c)	Total DPMO(c)	
SMT+ MVI	3,147	419	382	801	33
SMT+MVI +ICT	2,642	195	192	387	20
SMT+AXI+ICT	1,139	23	195	218	3

Table 2

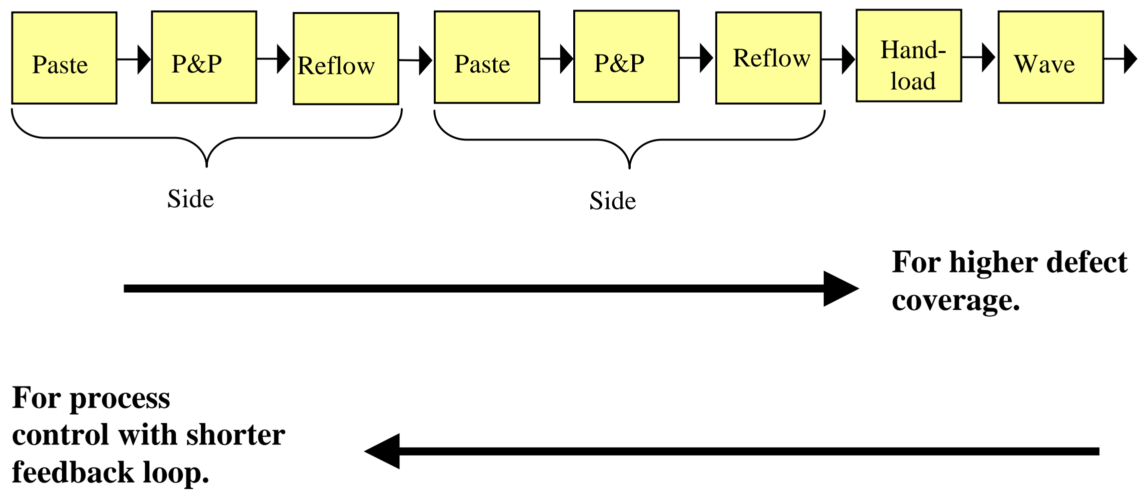

Figure 6. The basic concept of Automatic Inspection for process control versus defect containment.